EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	12	(Ching near Fai).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:10
S2	22	(Schumann near Steven).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:10
S3	28	(vikram near Kowshik).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:10
S4	56	S1 or S2 or S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:11
S5	1	S1 and S2 and S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:11
S7	5451993	(second 2w decoder)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:11
S8	263845	(bitline 2w decoder)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:12
S9	1378484	(synchron$4 2w reading)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:12
S10	82178	interleav$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:12

EAST Search History

S11	102742	odd and even	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:12
S12	114952	burst	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:12
S13	3832790	burst w controller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:12
S14	4942980	S6 and S7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 15:55
S15	262599	S8 and S14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 15:59
S16	113185	S9 and S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 15:59
S17	13640	S10 and S16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:00
S18	4007	S17 and S11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:00
S20	997867	column decoder	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:13
S21	667159	row decoder	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:13

EAST Search History

S22	374053	S20 and S21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:02
S23	3517	S19 and S22	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:02
S24	7991	(second adj2 decoder)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:12
S25	12	(Ching near Fai).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:11
S26	22	(Schumann near Steven).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:11
S27	28	(vikram near Kowshik).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:11
S28	12	(Ching near Fai).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:11
S29	22	(Schumann near Steven).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:11
S30	28	(vikram near Kowshik).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:11
S31	56	S28 or S29 or S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:11

EAST Search History

S32	1	S28 and S29 and S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:11
S33	8118	(first adj2 decoder)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:12
S34	136	(bitline adj2 decoder)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:20
S35	1606	(synchron$4 adj2 reading)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:14
S36	82178	interleav$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:12
S37	102742	odd and even	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:24
S38	114952	burst	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:12
S39	3832790	burst w controller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:16
S40	14495	column adj decoder	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:13
S41	15372	row adj decoder	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:13

EAST Search History

S42	5726	S24 and S33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:13
S43	6089	(synchron$4 adj2 read$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:21
S44	79	S42 and S43	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:14
S45	35	S44 and S36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:14
S46	13	S45 and S37	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:18
S47	13	S39 and S46	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:15
S48	10974	S40 and S41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:15
S49	0	S47 and S48	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:15
S50	161	burst adj controller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:18
S51	0	S46 and S50	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:18

EAST Search History

S52	892	(bit adj line adj2 decoder)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:20
S53	1016	S34 or S52	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:20
S54	10135	(synchron$4 near2 read$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:21
S55	14	S53 and S54	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:21
S56	1	S37 and S55	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:22
S57	1	S50 and S55	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:22
S58	3	S48 and S55	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:24
S59	3479015	odd or even or interleav$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:24
S60	196050	odd or interleav$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:24
S61	1	S55 and S60	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:25

EAST Search History

S62	0	S61 not S52	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:26
S63	2343	S54 and S60	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:26
S64	823	S38 and S63	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:27
S65	10974	S40 and S41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:27
S66	99	S64 and S65	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:28
S67	1	S66 and S50	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:28
S68	66309	(bit adj line) or bitline	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:28
S69	48	S66 and S68	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:29
S70	1033325	word$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:29
S71	704134	"48" and "49"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:29

EAST Search History

S72	47	S69 and S70	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:29
S73	783610	register$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:30
S74	40	S72 and S73	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:36
S75	2	first adj tier adj decoder	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:33
S76	1489	S37 and S63	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:36
S77	22	S37 and S74	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 16:36

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#1	((synchronous memory)<in>metadata)
#2	((synchronous or parallel or paralell) and reading<IN>metadata)
#3	(burst mode<IN>metadata)
#4	(burst controller<IN>metadata)
#5	(bitline decoder<IN>metadata)
#6	(column decoder<IN>metadata)
#7	((odd or even) and memory<IN>metadata)
#8	(column decoder<IN>metadata)
#9	(row decoder<IN>metadata)
#10	(((synchronous memory)<in>metadata)) <AND> ((burst mode<IN>metadata)) <AND> ((burst controller<IN>metadata))
#11	(((synchronous memory)<in>metadata)) <AND> ((burst controller<IN>metadata))
#12	(((synchronous memory)<in>metadata)) <AND> (((odd or even) and memory<IN>metadata))
#13	((((synchronous memory)<in>metadata)) <AND> (((odd or even) and memory<IN>metadata))) <AND> ((column decoder<IN>metadata))

Terms used
synchronous memory interleaving bitline decoder burst mode EDO dram

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1 A performance comparison of contemporary DRAM architectures

Vinodh Cuppu, Bruce Jacob, Brian Davis, Trevor Mudge

May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture ISCA '99**, Volume 27 Issue 2

Publisher: IEEE Computer Society, ACM Press

Full text available: pdf(166.88 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

In response to the growing gap between memory access time and processor speed, DRAM manufacturers have created several new DRAM architectures. This paper presents a simulation-based performance study of a representative group, each evaluated in a small system organization. These small-system organizations correspond to workstation-class computers and use on the order of 10 DRAM chips. The study covers Fast Page Mode, Extended Data Out, Synchronous, Enhanced Synchronous, Synchronous Link, Rambus, ...

2 Low power techniques for address encoding and memory allocation

Wei-Chung Cheng, Massoud Pedram

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Publisher: ACM Press

Full text available: pdf(110.42 KB)

Additional Information: full citation, abstract, references, citings, index terms

This paper presents encoding techniques to optimize the switching activity on a multiplexed DRAM address bus. The DRAM switching activity can be classified either as external (between two consecutive addresses) or internal (between the row and column addresses of the same address). To eliminate the external switching activity for sequential access, we propose an optimal encoding, Pyramid code, for conventional DRAM mode as well as Burst Pyramid code for burst mode DRAM. To minimize the inte ...

3 Low-energy off-chip SDRAM memory systems for embedded applications

Hojun Shim, Yongsoo Joo, Yongseok Choi, Hyung Gyu Lee, Naehyuck Chang

February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1

Publisher: ACM Press

Full text available: pdf(3.98 MB)

Additional Information: full citation, abstract, references, citings, index terms

Memory systems are dominant energy consumers, and thus many energy reduction techniques for memory buses and devices have been proposed. For practical energy reduction practices, we have to take into account the interaction between a processor and cache memories together with application programs. Furthermore, energy characterization of memory systems must be accurate enough to justify various techniques. In this article, we build an in-house energy simulator for memory systems that is accelerat ...

Keywords: Low power, SDRAM, memory system

4 Power reduction techniques for microprocessor systems

Vasanth Venkatachalam, Michael Franz
September 2005 **ACM Computing Surveys (CSUR)**, Volume 37 Issue 3
Publisher: ACM Press
Full text available: pdf(602.33 KB) Additional Information: full citation, abstract, references, index terms

Power consumption is a major factor that limits the performance of computers. We survey the "state of the art" in techniques that reduce the total power consumed by a microprocessor system over time. These techniques are applied at various levels ranging from circuits to architectures, architectures to system software, and system software to applications. They also include holistic approaches that will become more important over the next decade. We conclude that power management is a ...

Keywords: Energy dissipation, power reduction

5 Memory aware compilation through accurate timing extraction

Peter Grun, Nikil Dutt, Alex Nicolau
June 2000 **Proceedings of the 37th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(79.24 KB) Additional Information: full citation, abstract, references, citings, index terms

Memory delays represent a major bottleneck in embedded systems performance. Newer memory modules exhibiting efficient access modes (e.g., page-, burst-mode) partly alleviate this bottleneck. However, such features can not be efficiently exploited in processor-based embedded systems without memory-aware compiler support. We describe a memory-aware compiler approach that exploits such efficient memory access modes by extracting accurate timing information, allowing the compiler's sche ...

6 Processor-memory coexploration using an architecture description language

Prabhat Mishra, Mahesh Mamidipaka, Nikil Dutt
February 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 1
Publisher: ACM Press
Full text available: pdf(201.88 KB) Additional Information: full citation, abstract, references, index terms

Memory represents a major bottleneck in modern embedded systems in terms of cost, power, and performance. Traditionally, memory organizations for programmable embedded systems assume a fixed cache hierarchy. With the widening processor--memory gap, more aggressive memory technologies and organizations have appeared, allowing customization of a heterogeneous memory architecture tuned for specific target applications. However, such a processor--memory coexploration approach critically needs the ab ...

Keywords: Processor--memory codesign, architecture description language, design space exploration, memory exploration

7 Data and memory optimization techniques for embedded systems

P. R. Panda, F. Catthoor, N. D. Dutt, K. Danckaert, E. Brockmeyer, C. Kulkarni, A. Vandercappelle, P. G. Kjeldsberg

April 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 2

Publisher: ACM Press

Full text available: pdf(339.91 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a survey of the state-of-the-art techniques used in performing data and memory-related optimizations in embedded systems. The optimizations are targeted directly or indirectly at the memory subsystem, and impact one or more out of three important cost metrics: area, performance, and power dissipation of the resulting implementation. We first examine architecture-independent optimizations in the form of code transoformations. We next cover a broad spectrum of optimizati ...

Keywords: DRAM, SRAM, address generation, allocation, architecture exploration, code transformation, data cache, data optimization, high-level synthesis, memory architecture customization, memory power dissipation, register file, size estimation, survey

8 Low-voltage memories for power-aware systems

Kiyoo Itoh

August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(281.56 KB) Additional Information: full citation, abstract, references, citings

This paper describes low-voltage RAM designs for stand-alone and embedded memories in terms of signal-to-noise-ratio designs of RAM cells and subthreshold-current reduction.First, structures and areas of current DRAM and SRAM cells are discussed. Next, low-voltage peripheral circuits that have been proposed so far are reviewed with focus on subthreshold-current reduction, speed variation, on-chip voltage conversion, and testing.Finally, based on the above discussion, a perspective is given with ...

Keywords: DRAM and SRAM cells, gain cells, gate-source/substrate-source back-biasing, memory-rich architectures, multi-*Vr*, non-volatile RAMs, on-chip voltage converters, peripheral circuits, subthreshold current, testing

9 Energy-aware design of embedded memories: A survey of technologies, architectures, and optimization techniques

Luca Benini, Alberto Macii, Massimo Poncino

February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1

Publisher: ACM Press

Full text available: pdf(288.44 KB) Additional Information: full citation, abstract, references, index terms

Embedded systems are often designed under stringent energy consumption budgets, to limit heat generation and battery size. Since memory systems consume a significant amount of energy to store and to forward data, it is then imperative to balance power consumption and performance in memory system design. Contemporary system design focuses on the trade-off between performance and energy consumption in processing and storage units, as well as in their interconnections. Although memory design is as ...

Keywords: Embedded systems, embedded memories, integration, memories, nonvolatile,

system-on-a-chip, volatile

10 Power optimization and management in embedded systems

Massoud Pedram
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**
Publisher: ACM Press

Full text available: pdf(91.36 KB) Additional Information: full citation, abstract, references, citings, index terms

Power-efficient design requires reducing power dissipation in all parts of the design and during all stages of the design process subject to constraints on the system performance and quality of service (QoS). Power-aware high-level language compilers, dynamic power management policies, memory management schemes, bus encoding techniques, and hardware design tools are needed to meet these often-conflicting design requirements. This paper reviews techniques and tools for power-efficient embedd ...

11 Memory optimization for embedded systems: Memory layout techniques for variables utilizing efficient DRAM access modes in embedded system design

Yoonseo Choi, Taewhan Kim
June 2003 **Proceedings of the 40th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(198.61 KB) Additional Information: full citation, abstract, references, citings, index terms

The delay of memory access is one of the major bottlenecks in embedded systems' performance. In software compilation, it is known that there is high variations in memory access delay depending on the ways of storing/retrieving the variables in code to/from the memories. In this paper, we propose an effective storage assignment technique for variables to maximize the use of memory bandwidth. Specifically, we study the problem of DRAM memory layout for storing the non-array variables in code to ac ...

Keywords: embedded system, memory layout, page/burst modes, storage assignment

12 Low-power systems on chips (SOCs)

C. Piguet, M. Renaudin, T. Omnés
March 2001 **Proceedings of the conference on Design, automation and test in Europe**
Publisher: IEEE Press
Full text available: pdf(93.75 KB) Additional Information: full citation, references, index terms

13 Constructing application-specific heterogeneous embedded architectures from custom HW/SW applications

Steven Vercauteren, Bill Lin, Hugo De Man
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(97.89 KB) Additional Information: full citation, references, citings, index terms

14 Exploiting off-chip memory access modes in high-level synthesis

Preeti Ranjan Panda, Nikil D. Dutt, Alexandru Nicolau
November 1997 **Proceedings of the 1997 IEEE/ACM international conference on**

Computer-aided design
Publisher: IEEE Computer Society
Full text available: pdf(100.90 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Memory-intensive behaviors often contain large arrays that are synthesized into off-chip memories. With the increasing gap between on-chip and off-chip memory access delays, it is imperative to exploit the efficient access mode features of modern-day memories (e.g., page-mode DRAMs) in order to alleviate the memory bandwidth bottleneck. Our work addresses this issue by: (a) modeling realistic off-chip memory access modes for High-Level Synthesis (HLS), (b) presenting algorithms to infer applicab ...

Keywords: Memory Synthesis, DRAM, High Level Synthesis

15 Low-power embedded system design: Xtream-Fit: an energy-delay efficient data memory subsystem for embedded media processing
Anand Ramachandran, Margarida F. Jacome
June 2003 **Proceedings of the 40th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(246.05 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we propose a novel special-purpose data memory subsystem, called Xtream-Fit, aimed at achieving high energy-delay efficiency for streaming media applications. A key novelty of Xtream-Fit is that it exposes a single customization parameter, thus enabling a very simple and yet effective design space exploration methodology. A second key contribution of this work is the ability to achieve very high energy-delay efficiency through a synergistic combination of: (1) special purpose memor ...

Keywords: configurability, design space exploration, energy delay product, low power, media processing, scratch-pad, streaming memory

16 Concurrency, latency, or system overhead: which has the largest impact on uniprocessor DRAM-system performance?
Vinodh Cuppu, Bruce Jacob
May 2001 **ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual international symposium on Computer architecture ISCA '01**, Volume 29 Issue 2
Publisher: ACM Press
Full text available: pdf(904.17 KB) Additional Information: full citation, abstract, references, citings, index terms

Given a fixed CPU architecture and a fixed DRAM timing specification, there is still a large design space for a DRAM system organization. Parameters include the number of memory channels, the bandwidth of each channel, burst sizes, queue sizes and organizations, turnaround overhead, memory-controller page protocol, algorithms for assigning request priorities and scheduling requests dynamically, etc. In this design space, we see a wide variation in application execution times: for example, ...

17 Embedded software: Memory access driven storage assignment for variables in embedded system design
Yoonseo Choi, Taewhan Kim
January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design**

automation: electronic design and solution fair ASP-DAC '04
Publisher: IEEE Press , IEEE Press
Full text available: pdf(87.35 KB) Publisher Site Additional Information: full citation, abstract, references

It has been reported and verified in many design experiences that a judicious utilization of the page/burst access modes supported by DRAMs contributes a great reduction in not only the DRAM access latency but also DRAM's energy consumption. Recently, researchers showed that a careful arrangment of data variables in memory directly leads to a maximum utilization of the page/burst access modes for the variable accesses, but unfortunately, found that the problems are not tractable, consequently, r ...

18 Design space exploration for embedded systems: Energy exploration and reduction of SDRAM memory systems
Yongsoo Joo, Yongseok Choi, Hojun Shim, Hyung Gyu Lee, Kwanho Kim, Naehyuck Chang
June 2002 **Proceedings of the 39th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(196.08 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we introduce a precise energy characterization of SDRAM main memory systems and explore the amount of energy associated with design parameters, leading to energy reduction techniques that we are able to recommend for practical use.We build an in-house energy simulator for SDRAM main memory systems based on cycle-accurate energy measurement and state-machine-based characterizations which independently characterize dynamic and static energy. We explore energy behavior of the memory ...

Keywords: SDRAM, low power, memory system

19 Adaptive voltage scaling: Memory-aware energy-optimal frequency assignment for dynamic supply voltage scaling
Youngjin Cho, Naehyuck Chang
August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**
Publisher: ACM Press
Full text available: pdf(158.76 KB) Additional Information: full citation, abstract, references, index terms

Dynamic supply voltage scaling (DVS) is one of the best ways to reduce the energy consumption of a device when there is a super-linear relationship between energy and supply voltage, and a pseudo-linear relationship between delay and supply voltage. However, most DVS schemes scale the clock frequency of the supply-voltage-clock-scalable (SVCS) CPU only and do not address the energy consumption of the memory. The memory is generally non-supply-voltage-scalable (NSVS), but its energy consumption i ...

Keywords: SDRAM, low power, memory system

20 Session 6C: Markovian analysis and asynchronous circuits: Achieving fast and exact hazard-free logic minimization of extended burst-mode gC finite state machines
Hans Jacobson, Chris Myers, Ganesh Gopalakrishnan
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Press
Full text available: pdf(188.31 KB) Additional Information: full citation, abstract, references

This paper presents a new approach to two-level hazard-free logic minimization in the

context of extended burst-mode finite state machine synthesis targeting generalized C-elements (gC). No currently available minimizers for literal-exact two-level hazard-free logic minimization of extended burst-mode gC controllers can handle large circuits without synthesis times ranging up over thousands of seconds. Even existing heuristic approaches take too much time when iterative exploration over a large ...

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